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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/769,241 | 01/30/2004 | Mikhail A. Wolf | X-1334 US | 8159 |

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

| EXAMINER | |
|---|---|
| GUTIERREZ, ANTHONY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2857 | |

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/769,241 | WOLF, MIKHAIL A. | |
| | Examiner | Art Unit | |
| | Anthony Gutierrez | 2857 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruce, Jr. et al. (US Patent 5, 517, 637).

As to claims 1, 10, 11, 13-18, and 20, Bruce, Jr. et al., discloses a computer-implemented method and system for generating a test program for an integrated circuit design employing a boundary scan implementation, including a BSDL file generator, and including a plurality of boundary scan cells coupled to I/0 ports (Title, Abstract, and col. 1, lines 11-50), the method comprising: determining, from a netlist that describes the integrated circuit design, design information including the design architecture and type, name and direction of input and output ports used by the design (col. 3, lines 21-40); generating a current set of verilog test vectors from the design information; simulating the operation of the design using the current set of test vectors and storing result data output during the simulation; generating a new current set of test vectors as a function of the result data; repeating the steps of simulating, storing result data and generating a new current set of test vectors until selected completion criteria are satisfied (col. 4, lines 30-67 and Figs. 1 and 2); and in response to

the selected completion criteria being satisfied, generating the test program from the result data (col. 6, lines 9-21).

As to claims 2 and 8, Bruce, Jr. et al., discloses storing and using result data indicative of characteristics of design (col. 5, lines 56-65).

As to claim 3, Bruce, Jr. et al., discloses using the stored result data to determine circuit connectivity (col. 5, lines 42-55).

As to claims 4-7, and 9, Bruce, Jr. et al., discloses using the stored result data to map input and output boundary cells to boundary scan access ports (col. 1, lines18-50, and col. 3, line 41-col. 4, line 16, with respect to the discussion of the boundary scan register as it relates to the input/output, access ports, and cells).

As to claim 12, Bruce, Jr. et al., discloses generating new test vectors that use the identified circuit characteristics (See Fig. 2, boxes 208 and 216).

As to claim 19, Bruce, Jr. et al., discloses that the integrated circuit design includes at least two distinct circuits, each distinct circuit having test I/O ports and associated boundary scan cells coupled thereto, the plurality of boundary scan cells being coupled in a chain with output boundary scan cells from a first one of the at least two distinct circuits being coupled to input boundary scan cells of a second one of the at least two distinct circuits, wherein the storage circuit is adapted to store result data indicative of the chain connectivity of the output boundary scan cells to the input boundary scan cells and wherein the test program generator is adapted to generate the test program as a function of the chain connectivity (col. 1, lines 18-31)

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

*United States Patents*

US 6,721,923 B2 to Fisher, teaches a method for generating IC boundary register data by creating a boundary-scan description language file.

US 6,697,982 B2 to Chakravarthy et al., teaches a method for generating netlist test vectors by stripping references to a pseudo input.

US 6,560,739 B1 to Chung, teaches a mechanism for enabling compliance with IEEE standard 1149.1 for boundary scan designs and tests.

US 6,449,755 B1 to Beausang et al., teaches instruction signature and primary input and primary output extraction within an IEEE1149.1 compliance checker.

US 6,378,094 B1 to Chakraborty et al. teaches a method for testing cluster circuits in a boundary scan environment.

5,497,378 to Amini et al., teaches a method for testing a circuit network having elements testable by different boundary scan standards.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Gutierrez whose telephone number is (571) 272-2215. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AG
Anthony Gutierrez

6/24/05